

as 75% of the maximum output power. Stable operation up to 1600 h has been successfully demonstrated.

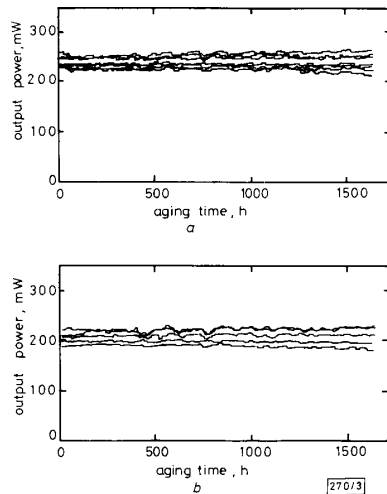


Fig. 3 Output powers as function of aging time for 1600 h at -40°C

Automatic current controlled (ACC) tests were used
a $1.3\ \mu\text{m}$ LDs ($I_d = 580 \sim 650\ \text{mA}$)
b $1.45\ \mu\text{m}$ LDs ($I_d = 440 \sim 550\ \text{mA}$)

Acknowledgment: We are indebted to Dr. Kawahara, Mr. Matoba and Ms. Oshiba for helpful discussions. We also thank Mr. Sakuta for his encouragement throughout this work.

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20th November 1989

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References

- OSHIBA, S., MATOBA, A., KAWAHARA, M., and KAWAI, Y.: 'High-power output over 200 mW of $1.3\ \mu\text{m}$ GaInAsP VIPS lasers', *IEEE J. Quantum Electron.*, 1987, **QE-23**, pp. 738-743
- HORIKAWA, H., OSHIBA, S., and KAWAI, Y.: 'V-grooved inner-stripe laser diodes on a p-type substrate operating over 100 mW at $1.5\ \mu\text{m}$ wavelength', *Appl. Phys. Lett.*, 1987, **50**, pp. 374-376
- OSHIBA, S., and KAWAI, Y.: 'High-power aging tests of 1.3 and $1.5\ \mu\text{m}$ VIPS lasers', *Electron. Lett.*, 1987, **23**, pp. 843-844
- OSHIBA, S., MATOBA, A., HORIKAWA, H., KAWAI, Y., and SAKUTA, M.: 'Reliability of $1.3\ \mu\text{m}$ V-grooved inner-stripe laser diodes under high-power operation', *ibid.*, 1986, **22**, pp. 428-429

SIZE LIMITS ON PHASED BURST ERROR CORRECTING ARRAY CODES

Indexing terms: Information theory, Codes and coding, Error-correction codes, Magnetic storage

A method for finding allowed array sizes for two-dimensional phased burst error correcting array codes is presented. These array codes have simple parity checks on two axes, have diagonal read-out, and are capable of correcting phased bursts along any one diagonal.

Simple two-dimensional array codes with modulo-two parity checks on both dimensions and diagonal read-out without skipping diagonals, introduced by Farrell and Hopkins,¹ have

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been shown to correct burst errors of length no more than the shorter dimension given that the array is rectangular with its length approximately twice its width. In particular, Blaum² has shown that to correct a burst of length $k_1 = n_1 - 1$, the second dimension $k_2 = n_2 - 1$ is constrained by

$$k_2 \geq 2(k_1 - 1) \quad (1)$$

In this letter we show that if the error is confined to a diagonal, the sizes of permissible arrays which are more square (and therefore have higher rate and allow more flexibility) can be found explicitly. Such codes have applications in silicon and magnetic data storage systems.

An array $n_1 \geq n_2$ cannot correct a phased burst of length n_1 , since if $n_1 = n_2$ a burst pattern of $(1, 1, \dots, 1)$ cannot be corrected, and since if $n_1 > n_2$ a burst pattern in the first position (starting at the first row of the first column) of the form $a_0, a_1, 0, \dots, 0, a_{n_2}, 0, 0, \dots$ where a_i are nonzero, cannot be distinguished from a burst pattern of $0, 1, 0, 0, \dots$ which occurs in the $n_2 - 1$ position (starting at the $n_2 - 1$ row position in the first column). However, an array $2n_1 \leq n_2$ can correct a phased burst because the vertical parities will always give the error pattern and the horizontal parities will have a string of $n_2 - n_1$ zeros where the error cannot exist; thus there is a unique set of n_1 parities which matches the error pattern and gives the error position. For $n_1 < n_2 < 2n_1$, the following theorem holds.

Theorem: If a burst error correcting array code exists, $n_1 < n_2 < 2n_1$, then

$$n_2 \neq \frac{\alpha + 1}{\alpha} (n_1 - \beta) \quad (2)$$

for all $\alpha \geq 1$ and $\beta \geq 1$. Moreover, this is a necessary and sufficient condition for the code to exist.

Proof: A burst of errors is miscorrected when its position is found erroneously. The vertical parities specify the burst pattern and are therefore unique for each error pattern. The horizontal parities, together with this error pattern, provide the position. Therefore, when the error pattern is such that two positions can have the same horizontal parity check sums, then decoder error occurs.

There are many classes of error patterns which fit into this category. A symbolic representation of these is shown in Fig. 1. Here x denotes the length of the section with a not-all-zero pattern and a and b denote the length of the sections with all zeros. There are α sections of b and $\alpha + 1$ sections of x in the burst of length n_1 ; an all-zero section of length c has been added to the front to make the length of the burst equal to n_1 . A shift of $e = x + b$ results in a horizontal parity check pattern indistinguishable from the original.

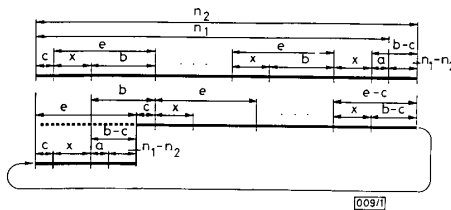


Fig. 1 Symbolic representation of original and shifted burst patterns

Note that the case where the shift is $2e$ or some larger multiple of e is also possible. However, such a shift is only indistinguishable if the original shift of e is indistinguishable; therefore, this case need not be addressed separately. From the Figure, the following relations can be found:

$$n_2 = (\alpha + 1)(x + b) \quad (3)$$

$$b = e - x = c + a + n_2 - n_1 \quad (4)$$

Combining these yields

$$n_2 = \frac{\alpha + 1}{\alpha} [n_1 - (x + c + a)] \quad (5)$$

Because $x \geq 1$, $c \geq 0$ and $a \geq 0$, the factor $x + c + a$ can be compressed into one term β , $\beta \geq 1$, so that

$$n_2 = \frac{\alpha + 1}{\alpha} (n_1 - \beta) \quad (6)$$

These are the values of n_2 which cannot be used by the code, or else there may be two errors with the same parity patterns. Therefore, that a phased burst error correcting array code cannot have these values of n_2 is proven.

That this condition is sufficient remains to be argued. Consider that any error pattern which is in the form described above must allow the resulting horizontal parity check pattern to be identical to that of the same pattern in a different position, and is therefore one period (or more) lagging or leading because of the periodicity of the index (taken modulo n_2). That is, by adding $n_2 - n_1$ zeros to the end of the error pattern, the error pattern must become periodic. The pattern must have two or more full periods represented when the $n_2 - n_1$ zeros are appended to it, and no partial cycles are permitted. All 'periodic' error patterns have been covered. Therefore, for the condition to be sufficient, there must be no non-'periodic' error patterns which can lead to erroneous decoding.

Non-'periodic' patterns have nonrepeating patterns over the positions $0 \leq i \leq n_2 - 1$ where the positions beyond the first n_1 are stuffed with all zeros. The period is therefore now n_2 , and the 'phase', i.e. the position, of the error can be determined uniquely. Therefore, no non-'periodic' error patterns can result in erroneous decoding.

Table 1 ALLOWED VALUES FOR n_2 GIVEN n_1

n_1	Allowed n_2 , $n_2 < 2n_1$	n_1	Allowed n_2 , $n_2 < 2n_1$
2	3	10	11, 13, 15, 17, 19
3	5	11	13, 17, 19, 21
4	5, 7	12	13, 17, 19, 21, 23
5	7, 9	13	17, 19, 21, 23, 25
6	7, 9, 11	14	17, 19, 21, 23, 25, 27
7	11, 13	15	17, 19, 23, 25, 27, 29
8	11, 13, 15	16	17, 19, 23, 25, 27, 29, 31
9	11, 13, 15, 17	17	19, 23, 25, 27, 29, 31, 33

The theorem provides a means of more flexibly constructing single phased burst error correcting array codes of higher rate by decreasing the number of parity check bits needed. A square array provides the highest rate for the number of information bits it holds. Some allowed sizes of codes are listed in Table 1. Note that only values for $n_2 < 2n_1$ are listed; other array sizes do not do better than the general burst error correcting array code. Computer simulation tests have confirmed these results.

A comparison of rates for codeword size has been plotted between the general burst error correcting code and this code in Fig. 2. The difference is small for large codewords, but for

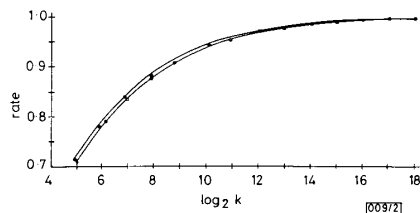


Fig. 2 Comparison of rates between general and phased burst error correcting array codes for various codeword sizes

—○— Farrell burst ECC¹ —●— phased burst ECC

codewords of 1024 bits or less or for computer memories where even slight improvements in rate are welcome, the phased burst error correcting code is advantageous.

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5th October 1989

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References

- 1 FARRELL, P. G., and HOPKINS, S. J.: 'Burst-error-correcting array codes', *Radio & Electron. Eng.*, April 1982, **52**, (4)
- 2 BLAUM, M.: 'Error-correcting codes for computer memories'. PhD thesis, California Institute of Technology, 1985
- 3 GOODMAN, R. M., and SAYANO, M.: 'On-chip ECC for multi-level random access memories'. IEEE workshop on information theory, Cornell University, Ithaca, NY, 26th-29th June 1989

GaAs PHOTOCONDUCTOR ARRAY AS NEW DETECTOR IN MULTICHANNEL SPECTROSCOPIC SYSTEM

Indexing terms: Optoelectronics, Photoconducting devices, Photodetectors, Spectroscopy

We introduce a new linear array of GaAs planar photoconductive detectors for multichannel applications. After a description of the device, its electrical properties are described in terms of its specific detectivity. Then, the results of a performance test of the photoconductor array as a detection system in a multichannel Raman spectrometer are presented.

Recently it has been shown that carefully designed N -type GaAs planar photoconductors present high detectivity values, close to $10^{13} \text{ cm}^2/(\text{Hz W}^{-1})$.¹ Because such devices have specific detectivity values similar to those of photomultiplier tubes, it is of interest to estimate their performance in spectroscopic systems. Tests of these devices have been carried out in a conventional Raman instrument, and indicate that they are advantageous alternatives to photomultiplier tubes in DC spectroscopic detection systems.²

The next step in this work was the determination of the performance characteristics of N -type GaAs planar photoconductor arrays for the detection of low light power levels in multichannel spectroscopic systems. This application has led to the development of a photoconductor array associated with an appropriate electronic circuit for use in a Raman multichannel spectrometer.

The photoconductor array was fabricated in our laboratory with the use of epitaxies suitable for FETs, with respect to the following requirements: (i) the doping level and the depth of the photoconductive layer have been chosen to minimise the dark current; (ii) photosensitive elements have been associated with dummy elements to cancel the dark current; and (iii) the elements have been electrically isolated from each other.

The schematic arrangement and a photomicrograph of the array are given in Fig. 1a and Fig. 2, respectively. The device is composed of series of photosensitive and dummy elements. The geometry has been chosen to fit the slit of a spectrometer. The photosensitive area ($10 \mu\text{m} \times 100 \mu\text{m}$) of each element is localised between two electrodes. Each electrode which collects the photocurrent has dimensions of $3 \mu\text{m} \times 100 \mu\text{m}$. The isolation mesa between two adjacent elements is $3 \mu\text{m} \times 100 \mu\text{m}$. Thus, the spatial resolution of the photoconductor array is $19 \mu\text{m}$, a value which is smaller than, for example, the spatial resolution ($25 \mu\text{m}$) of a Reticon Si photodiode array.

The schematic representation of photosensitive and dummy elements is given in Fig. 1b. The GaAs epitaxy has been spe-